CLAIMS

1. A method of relieving charge accumulations from non-volatile memory structures on dies on a wafer, including:

applying an electrical erase signal to the non-volatile memory structures on the dies; and

baking the wafer under conditions sufficient to diffuse charges resulting from the erase signal.

2. The method of claim 1, wherein the electrical erase signal produces a negative gate channel erase by Fowler-Norheim tunneling.

3. The method of claim 1, wherein the electrical erase signal produces a negative gate source side erase by Fowler-Norheim tunneling.

4. The method of claim 1, wherein the electrical erase signal produces a hot hole erase.

5. The method of claim 4, wherein the hot hole erase includes biasing either a source or drain of the memory cells.

6. The method of claim 4, wherein the hot hole erase includes biasing both of a source and drain of the non-volatile memory cells.

7. The method of claim 1, wherein the non-volatile memory structures include an ONO structure.

8. The method of claim 7, wherein the electrical erase signal produces a hot hole erase.

9. The method of claim 8, wherein the hot hole erase includes biasing either a source or a drain of the memory cells.

10. The method of claim 8, wherein the hot hole erase includes biasing both a source and a drain of the non-volatile memory cells.

11. The method of claim 1, wherein the baking includes heating the wafer to between 80 and 150 degrees Celsius.

12. The method of claim 1, wherein the baking includes heating the wafer to between 150 and 250 degrees Celsius.

13. The method of claim 1, further including determining an erasure state of the memory cells and repeatedly applying an additional electrical erase signal until a predetermined erasure state is achieved.

14. A method of relieving charge accumulations from ONO non-volatile memory structures on dies on a wafer, including applying an electrical erase signal to the ONO non-volatile memory structures on the dies prior to subdividing the wafer into the dies.

15. The method of claim 14, further including baking the wafer after applying the electrical erase signal under conditions sufficient to diffuse charges resulting from the electrical erase signal.

16. The method of claim 15, wherein the baking includes heating the wafer to between 80 and 150 degrees Celsius.

17. The method of claim 15, wherein the baking includes heating the wafer to between 150 and 250 degrees Celsius.

18. The method of claim 14, wherein the electrical erase signal produces a negative gate channel erase by Fowler-Norheim tunneling.

19. The method of claim 14, wherein the electrical erase signal produces a negative gate source side erase by Fowler-Norheim tunneling.

20. The method of claim 14, wherein the electrical erase signal produces a hot hole erase.

21. The method of claim 20, wherein the hot hole erase includes biasing either a source or a drain of the memory cells.

22. The method of claim 20, wherein the hot hole erase includes biasing both a source and a drain of the non-volatile memory cells.

23. The method of claim 22, further including determining an erasure state of the memory cells and repeatedly applying an additional electrical erase signal until a predetermined erasure state is achieved.